CBCS SCHEME

USN | | | | | | | | | | |

15EC53

Fifth Semester B.E. Degree Examination, July/August 2021
Verilog HDL

Time: 3 hrs. Max. Marks:80

Note: ***Answer any FIVE full questions.***

1 a. Explain a typical design flow for designing VLSI IC circuit using block diagram. **(06 Marks)**

b. Develop virolog code for 4-bit ripple carry counter and with neat block diagram explain design hierarchy for the same. **(10 Marks)**

2 a. Explain to-down design methodology and bottom up design methodology. **(10 Marks)**

b. Explain the importance of HDL and also mention useful features of verilog HDL. **(06 Marks)**

3 a. Explain the following data-types with an example in verilog :
i) Nets ii) Registers iii) Vectors iv) Arrays. **(08 Marks)**

b. Explain the below mentioned system tasks NAND complier directives with examples :
i) $display ii) $monitor iii) 'Define iv) 'Include. **(08 Marks)**

4 a. With a neat block diagram explain components of verilog module. **(06 Marks)**

b. Explain part connection rules. **(06 Marks)**

c. Write a verilog code for SR latch using and gates as elements. **(04 Marks)**

5 a. What are rise, fall and turnoff delays? How they are specified in verilog. **(06 Marks)**

b. Design and develop verilog code for an 4-bit ripple carry adder using 1-bit fulladder as a component. Also write stimulus for 4-bit ripple carry fulladder. **(10 Marks)**

6 a. For the schematic network shown below. Write a verilog code for gate level implementation with delay s mentioned :

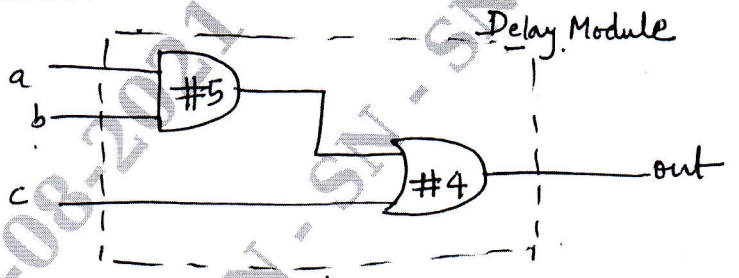

Fig.Q6(a)

Also write stimulus for the above example. **(06 Marks)**

b. Write a verilog code for :
i) 2 : 1 mux with conditional operator
ii) 4 : 1 mux with conditional operators
iii) 4 : 1 mux using logic equation
iv) 2 : 1 mux using logic equation. **(10 Marks)**

7 a. Explain with examples always and initial statements. **(08 Marks)**

b. Explain blocking assignment statements and non-blocking assignment statements with relevant examples. **(08 Marks)**

8 a. Explain sequential and parallel blocks with examples. **(08 Marks)**

b. Write a verilog code for :

i) 4 : 1 multiplexer using case statement

ii) 4 – bit counter with behavioral description. **(08 Marks)**

9 a. Explain design tool flow diagram with block diagram. **(08 Marks)**

b. i) Write VHDL dataflow description for – 4 – bit equality comparator using logic equations and block diagrams. **(04 Marks)**

ii) Write VHDL structural description for 4-bit comparator with necessary block diagrams. **(04 Marks)**

10 a. Explain the declaration of constant, variable and signal in VHDL, with example. **(08 Marks)**

b. Explain attributes in VHDL. **(04 Marks)**

c. Write a VHDL code for half adder using behavioral description. **(04 Marks)**

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